IN THE CLAIMS:

1. (Currently Amended) A self orthogonal ~~code~~ decoding circuit <u>for</u> ~~performing~~ decoding ~~for~~ <u>a</u> self orthogonal code <u>and</u> repeating decoding ~~for~~ <u>of</u> said self orthogonal code for a plurality of times, <u>using a plurality of decoding stages, wherein for each of said plurality of stages, a reception series error detection threshold value for detecting a reception series error is set to a predetermined value and in a first decoding stage, said reception series error detection threshold value is set high for detecting a reception series error only if there is a high probability of error and the threshold values are gradually lowered in each successive decoding stage, for error detection when there is a lower probably of error.</u>

2. (Currently Amended) A self orthogonal <u>code</u> decoding circuit <u>for</u> ~~performing~~ decoding for <u>a</u> self orthogonal code on the basis of a syndrome bit determined ~~only~~ by an error in a reception series which ~~is~~ <u>was</u> generated ~~by adding error to~~ <u>from</u> a transmission series, which ~~is~~ <u>was</u> in turn generated by <u>a</u> parallel/serial conversion ~~with~~ <u>and by</u> adding a check series to an information series, comprising:

       a plurality of <u>decoding circuit</u> stages ~~of deciding circuit~~ for repeating decoding ~~for~~ <u>of</u> said self orthogonal code ~~for~~ <u>a</u> plurality of times; and

       <u>a</u> check series register <u>output</u> provided ~~for~~ <u>from</u> each decoding circuit <u>stage</u> except ~~for the~~ <u>from a final</u> decoding circuit <u>stage,</u> ~~at a final stage among said plurality of stages of decoding circuits and~~ for inputting said check series to <u>the</u> next ~~stage of~~ decoding circuit <u>stage</u> with <u>a</u> delay.

3. (cancelled)

4. (Currently Amended) A self orthogonal <u>code</u> decoding circuit as set forth in claim ~~2~~ <u>1</u>, which comprises means for performing <u>a</u> code synchronization ~~judgment~~ <u>error detection</u> by counting <u>the</u> number of <u>detected reception series</u> errors ~~as being judged as error~~ and performing code synchronization <u>error detection</u> on the basis of <u>the</u> counted ~~error~~ number <u>of detected errors</u>.

5. (Currently Amended) A self orthogonal <u>code</u> decoding circuit as set forth in claim ~~3~~ <u>1</u>, which comprises <u>a</u> code synchronization dedicated ~~threshold value judgment~~ <u>error detection</u> circuit provided separately from ~~the~~ <u>a</u> circuit for ~~making judgment of~~ said <u>reception series</u> error <u>detection</u> ~~and dedicated for code synchronization and making judgment whether~~ <u>for detecting a synchronization</u> error ~~is caused or not~~ on the basis of ~~threshold value judgment~~ <u>a</u> threshold value optimized for code synchronization <u>error detection,</u> ~~and said threshold value of~~ said code synchronization dedicated <u>error detection</u> threshold value ~~judgment circuit to be~~ being lower than said ~~threshold value~~ <u>reception series</u> error ~~judgment~~ <u>detection</u> threshold value.

6. (Currently Amended) A self orthogonal <u>code</u> decoding circuit as set forth in claim 5, which comprises a syndrome register which shifts said syndrome bit ~~provided for code synchronization to output~~ to said code synchronization dedicated ~~threshold value judgment~~ <u>error detection</u> circuit, so as not to perform <u>reception series error</u> correction on the basis of <u>the</u> <u>result of</u> error ~~judgment of~~ <u>detection by</u> said code synchronization dedicated ~~threshold value judgment~~ <u>error detection</u> circuit ~~for said syndrome register~~.

3   G:\NEC\1084\14954\amend\14954.am1.rtf

7. (Currently Amended) A self orthogonal <u>code</u> decoding circuit as set forth in claim 4,

wherein each decoding circuit in said plurality <u>of</u> stages comprises:

<u>a</u> syndrome generation means for generating said syndrome bit;

<u>an</u> error value generation means for ~~leading~~ <u>generating</u> an error value by ~~making~~

~~judgment of~~ <u>detecting an</u> error of said syndrome bit generated by said syndrome generation

means<u>,</u> on the basis of said <u>reception series error detection</u>

threshold value ~~judgment threshold value~~

<u>an</u> error correcting means for correcting <u>an</u> error of said syndrome bit on the basis of

said error value generated by said error value generation means; and

<u>an</u> error detection counter for counting errors on the basis of said error value

generated by said error value generation means.

8. (Currently Amended) A self orthogonal <u>code</u> decoding circuit as set forth in claim 1,

~~wherein~~, in a system including

an information source generating an information series,

an encoder for converting said information series into a code series, and

a communication path for transmitting said code series~~, decoding for said self~~

~~orthogonal code is repeated for a plurality of times~~.

9. (Currently Amended) A self orthogonal <u>code</u> decoding circuit as set forth in claim 8,

wherein said communication path is constructed with a wired cable.

10. (Currently Amended) A self orthogonal <u>code</u> decoding circuit as set forth in claim 9,

wherein said wired cable is an optical cable.

11. (Currently Amended) A self orthogonal <u>code</u> decoding circuit as set forth in claim 8,

wherein said communication path is a transmission path in radio communication.

12. (Currently Amended) A self orthogonal <u>code</u> decoding method for ~~performing~~

decoding ~~for~~ <u>of</u> a self orthogonal code <u>and</u> repeating decoding ~~for~~ <u>of</u> said self orthogonal

code ~~for~~ a plurality of times, <u>using a plurality of decoding stages, wherein for each of said</u>

<u>plurality of stages, a reception series error detection threshold value for detecting a reception</u>

<u>series error is set to a predetermined value and in a first decoding stage, said reception series</u>

<u>error detection threshold value is set high for detecting a reception series error only if there</u>

<u>is a high probability of error and the threshold values are gradually lowered in each</u>

<u>successive decoding stage, for error detection when there is a lower probably of error.</u>

13. (Currently Amended) A self orthogonal <u>code</u> decoding method <u>for</u> ~~performing~~

decoding ~~for~~ <u>a</u> self orthogonal code on the basis of <u>a</u> syndrome bit determined ~~only~~ by an

error in a reception series which ~~is~~ <u>was</u> generated ~~by adding error to~~ <u>from</u> a transmission

series which ~~is~~ <u>was</u> in turn generated by <u>a</u> parallel/serial conversion ~~with~~ <u>and by</u> adding ~~an~~ <u>a</u>

check series to an information series, comprising a step of:

in each of a plurality of <u>decoding circuit</u> stages ~~of deciding circuit~~ for

repeating decoding ~~for~~ <u>of</u> said self orthogonal code <u>for</u> a plurality of times, said check series

~~being~~ <u>is</u> input to <u>a</u> next <u>decoding circuit</u> stage ~~of decoding circuit~~ with a delay<u>,</u> except ~~for~~

from the ~~decoding circuit at the~~ final <u>decoding circuit</u> stage.

14. (cancelled)

15. (Currently Amended) A self orthogonal <u>code</u> decoding method as set forth in claim ~~13~~ <u>12</u>, which comprises means for performing code synchronization ~~judgment~~ <u>error detection</u> by counting <u>the</u> number of <u>detected reception series</u> errors ~~as being judged as error~~ and performing code synchronization <u>error detection</u> on the basis of <u>the</u> counted ~~error~~ <u>number of errors</u>.

16. (Currently Amended) A self orthogonal <u>code</u> decoding method as set forth in claim 15, wherein a threshold value of a code synchronization dedicated ~~threshold value judgment~~ <u>error detection</u> circuit <u>is</u> provided separately from the circuit for ~~making judgment of said error~~ <u>reception series error detection</u> and dedicated ~~for~~ <u>to</u> code synchronization <u>error detection</u> ~~and making judgment whether error is caused or not~~ on the basis of ~~threshold value judgment~~ <u>a</u> threshold value optimized for code synchronization~~,~~ <u>error detection</u> being set lower than said <u>reception series error detection</u> threshold value ~~judgment threshold value~~.

17. (Currently Amended) A self orthogonal <u>code</u> decoding method as set forth in claim 16, which comprises a step of providing a syndrome register which shifts said syndrome bit ~~provided for code synchronization to output~~ to said code synchronization dedicated ~~threshold value judgment~~ <u>error detection</u> circuit, so ~~as~~ not to perform <u>reception series</u> error correction on the basis of the result of error <u>detection by</u> ~~judgment of~~ said code

6   G:\NEC\1084\14954\amend\14954.am1.rtf

synchronization dedicated ~~threshold value judgment~~ <u>error detection</u> circuit ~~for said~~

~~syndrome register.~~

18. (Currently Amended) A self orthogonal <u>code</u> decoding method as set forth in claim 15, which includes

      ~~step of~~ generating said syndrome bit,

      ~~step of leading~~ <u>generating</u> an error value by ~~making judgment of~~ <u>detecting an</u> error of said syndrome bit generated by said syndrome generation means on the basis of said ~~threshold value judgment~~ <u>reception series error detection</u> threshold value,

      ~~step of~~ correcting <u>the</u> error of said syndrome bit on the basis of said error value generated by said error value generation means;

      and ~~step of~~ counting said error number on the basis of said error value generated by said error value generation means.

19. (Currently Amended) A self orthogonal <u>code</u> decoding method as set forth in claim 12, ~~wherein,~~ in a system including

      an information source <u>for</u> generating an information series,

      an encoder for converting said information series into a code series, and

      a communication path for transmitting said code series~~, decoding for said self orthogonal code is repeated for a plurality of times~~.

20. (Currently Amended) A self orthogonal <u>code</u> decoding method as set forth in claim 19, wherein said communication path is constructed with a wired cable.

21. (Currently Amended) A self orthogonal <u>code</u> decoding method as set forth in claim 20, wherein said wired cable is an optical cable.

22. (Currently Amended) A self orthogonal <u>code</u> decoding method as set forth in claim 19, wherein said communication ~~oath~~ <u>path</u> is a transmission path in radio communication.